

# **Z-Interconnect Technology - A Reliable, Cost Efficient Solution for High Density, High Performance Electronic Packaging**

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## **Abstract**

Common themes across all segments of electronic packaging today are density and performance. High density interconnect (HDI) technology is one of the most commonly utilized methods for electronic package density improvement, while many different areas have been investigated for performance improvement, from low loss dielectric and conductor materials, to via design and via stub reduction. Electrical performance and density requirements are sometimes complementary, but often times, conflicting with one another.

This paper will describe the design, materials, fabrication, and reliability of a new Z-Interconnect technology that addresses both high density and high performance demands simultaneously. Z-Interconnect technology uses an electrically conductive adhesive to electrically interconnect several cores (Full Z) or sub-composites (Sub Z) in a single lamination process. Z-Interconnect technology will be compared and contrasted to other commonly used solutions to the performance and density challenges. HDI or sequential build-up technology is a pervasive solution to the density demands in semiconductor packaging and consumer electronics (e.g. Smart phones), but has not caught hold in HPC or A&D printed wiring board (PWB) applications. One solution for PWB electrical performance enhancement is plated through hole (PTH) stub reduction by “back drilling” the unwanted portion of the PTH.

Pb-free reflow and Current Induced Thermal Cycling (CITC) test results of product coupons and specially designed test vehicles, having component pitches down to 0.4mm, will be presented. Z-Interconnect test vehicles have survived 6X Pb-free (260C) reflow cycles, followed by greater than 3000 cycles of 23C-150C CITC cycles. Test vehicle and product coupons also easily survive 10 or more 23C-260C CITC cycles.

## **Key words**

Z-interconnect, density, electrically conductive adhesive, electrical performance, reliability

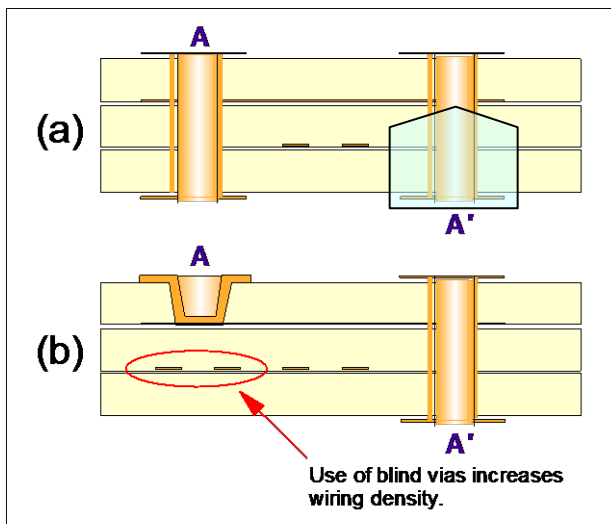
## **I. Introduction**

The ever increasing demands for data volume and speed are driving a convergence of electronic packaging density and performance across many diverse applications. The drive for high density is evident in semiconductor packaging and handheld devices, where high I/O 0.4mm BGA, die stacking and package stacking are all becoming commonplace. High Density Interconnect (HDI) technology is also highly utilized in semiconductor packaging and handheld device applications. Common solutions for high performance / high speed applications such as high performance computing (HPC) are low loss dielectric materials, reduced roughness conductors, wider traces and reduction or elimination of discontinuities and reflections in the signal path, such as by via size reduction and via stub elimination. As will be described in further detail

below, high density and high performance can often be conflicting objectives. This paper will describe the design, materials, processes and reliability test results of a new electronic packaging technology, Z-Interconnect, which can provide a common, cost effective solution for the competing objectives of density and performance. The primary focus of the paper will be on Full Z technology, where one to four layer cores are fabricated separately, in parallel, and then bonded together, using an electrically conductive adhesive (ECA), in a single final lamination step to interconnect the layers in the desired configuration. Limited test data will be presented on Sub Z, where sub-composites containing four or more circuit layers, are bonded together with an ECA to form the final composite structure.

### II.A. High Density Interconnect (HDI) Technology

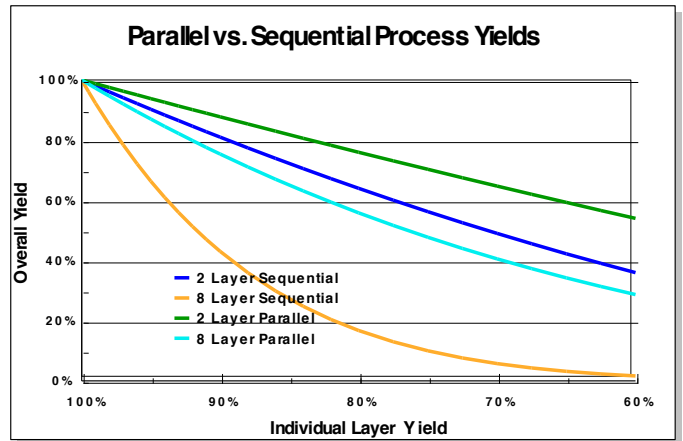
HDI technology has been commonplace in semiconductor packaging and handheld device (e.g. smart phones) since the mid 1990's. Adding wiring layers is a straightforward means of providing greater density and function in the package. However, adding layers invariably translates to added cost. It is therefore imperative to make the most efficient use of real estate used for wiring in order to keep the number of wiring layers to a minimum. Packaging designs that are most effective in optimizing the use of available wiring space incorporate blind and buried vias. For interconnection with traditional PTH technology, two PTHs are required to complete a circuit trace. PTHs consume real estate by blocking channels that could be used for wiring (**Figure 1**). HDI technology is a sequential process method of bonding dielectric and conductor layers onto a core or sub-composite, then drilling blind vias, plating / circuitizing to achieve the final circuit structure. To achieve even higher densities conductor width and dielectric thickness are reduced and more sequential build-up layers are added. Trace widths of 25 microns or less and via diameters of 50 micron and less are commonly used. Three (3+3) or four (4+4) sequential build-up layers per side are commonly used, with some applications looking to five and even six (6+6) build-up layers per side. The highest densities are achieved with a "coreless" structure, where the smallest via pitch can be utilized throughout the stack-up, as via diameter is not limited by plating aspect ratio.



**Figure 1:** Conventional plated through holes block wiring channels throughout stack-up (1a). The use of blind vias increases wiring density in circuit layers below the via (1b). The further impact of back drill is also illustrated in 1(a) A'.

A primary drawback of HDI technology is the cost associated with the cumulative effect of yield (**Figure 2**). Other drawbacks of HDI technology can be long fabrication

cycle times due to the sequential processing, thermal degradation of the laminate material and interfaces after multiple lamination cycles and limited application to high-performance applications, as dielectric material types and thickness are often limited by either supply or plating aspect ratio demands. On the other hand, HDI technology can provide truly stub-less, high performance vias in a coreless structure.



**Figure 2:** Cumulative effect of yield with sequential processing.

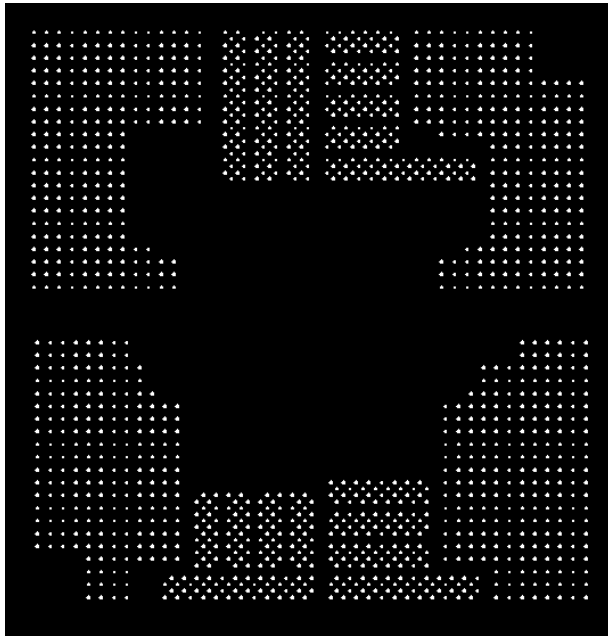
### II.B. Via Stub Elimination – Back drill

Back drilling, as a means of via stub elimination or reduction, is becoming more prevalent in recent years for HPC PWB backplane or midplane applications. In conventional PWB technology, signal and power core layers are built in parallel, then the layers are stacked and bonded together, holes are then drilled through the stack and copper plated to electrically interconnect the various layers. A typical high performance circuit will have traces routed on one of the internal layers of the PWB, and will be interconnected to components on the surface of the board via PTH's. The PTH that extends beyond the target internal wiring layer is referred to as a via stub. These via stubs can cause unwanted reflections in the transmission line.

One HPC PWB application recently encountered contains 44 total layers, with 14 of these being tri-plate (G-S-G) internal signal layers. This particular application contains approximately 50,000 PTH's with 13,000 of them requiring back drill. Back drill is required to multiple depths from both sides of the board. A typical BGA module on this PWB contains approximately 3800 PTH's, with 1500 requiring back drill (**Figure 3**). The intense back drill requirements of this particular application drove a module I/O pitch increase from 1.0mm up to 1.06mm, in order to accommodate differential pair escape.

The drawbacks of back drill should become readily apparent:

1. Reduced density over PTH alone due to the reduced channel width from the increased back drill diameter.
2. Yield / cost impacts of a bad back drill – too deep, not deep enough, broken drill, clipped trace, etc.
3. Potential reliability impact [1]. One potential reliability impact is back drilling only marginally too deep, which could compromise the inner plane connection.
4. Inability to effectively measure remaining stub length
5. Cost impacts of larger module pitch and added PWB circuit layers due to reduced density of back drill.

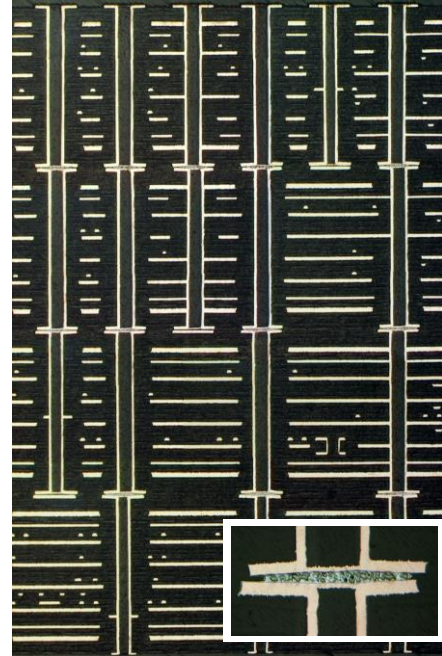


**Figure 3:** 1500 Back drills within a 3800 I/O module site for a 44 layer HPC PWB.

### II.C. Sub-composite Z-Interconnect (Sub Z) Technology

A first approach to the issues of high density combined with high performance is Sub Z. This is a technology that has been utilized for some of the more demanding applications at i3 electronics for the past several years. In Sub Z technology, the PWB stack is divided into more manageable pieces or sub-composites, the sub-composites are fabricated and electrically tested in parallel, then the sub-composites are conductively bonded together in a final lamination step. In one particular application (**Figure 4**), a 0.4" thick, 72 layer board was divided into four 0.1" thick, 18 layer sub-composites. This type of board, which would be nearly impossible to build by conventional methods due to the 0.008" drill diameter (~50:1 aspect ratio), has been running in production at high yield. As can be seen in **Figure 4**, this type of construction provides several advantages towards the high density, high performance objectives. There is a significant increase in wiring density in the lower subs, where vias have been terminated in the upper subs. Performance

benefits are achieved because the via stub length is limited to somewhat less than the thickness of the sub and the via itself can be smaller diameter than if it were through the entire board, leading to reduced via impedance discontinuity and wider wiring channels that can provide wider trace widths and smaller power plane clearances, providing better power integrity (PI).



**Figure 4:** Sub Z board, containing 4 subs, 3 Z-I joint layers, ~220,000 total joints.

There are some limitations with Sub Z, as it does not provide maximum density of HDI, as vias still pass through several layers creating wiring channel blockages. The via diameter must be sufficiently large to stay within manufacturable aspect ratio limitations. Of course, the long sub vias also will have via stubs, unless they are combined with back drill stub elimination. Perhaps the most significant limitation is limited extendibility below 0.8mm grid / BGA pitch. This limitation is due to the Z-Interconnect pad and space dimensions that are utilized to provide the most robust and reliable joint.

The limitations of HDI, back drill and Sub Z that have been detailed above, regarding density, performance and cost, have lead to the development of Full Z technology [2]. The objectives of Full Z technology were to optimize density and performance, while maintaining interconnect reliability and comparable cost.

### III. Full Z-Interconnect (Full Z) Technology

Full Z technology utilizes a joining core concept to interconnect signal and power cores to allow any layer via

interconnect, or connection between any two layers in the PWB stack, without any via stubs. (Figure 5).

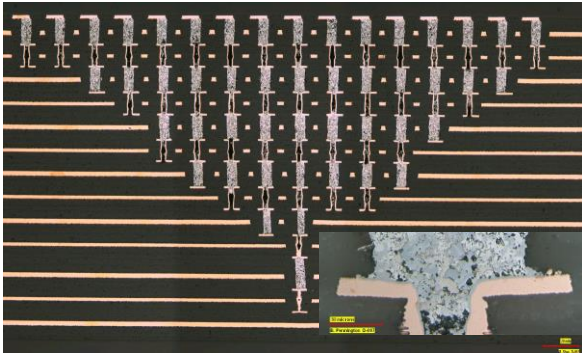


Figure 5: 0.5mm BGA module x-section from a 27 layer test vehicle.

### III.A. Full Z Design

Preferred cores for Full Z technology are 2S1P (two signals, one power in a signal-power-signal configuration) and 0S1P (no signals, one power) joining cores. This type of construction allows for full tri-plate (ground-signal-ground) wiring while the center plane layer provides dimensional stability and controlled CTE for each individual core and enables extension to glass-less PWB's. Other types of cores that have been demonstrated include 2S0P, 1S1P, 0S3P and 0S0P joining cores.

2S1P and 0S1P laser or mechanically drilled via dimensions down to 100 microns (0.004") with 250 micron (0.010") lands and 300 micron clearance lands have been demonstrated in PWB's, enabling via / BGA pitches of 0.4mm. 50 micron via dimensions have been demonstrated in Full Z semiconductor chip packages, providing for 150 micron C4 pitch escape (Figure 6). The smaller via dimensions utilized here minimize the trace to via impedance discontinuities, making the via virtually transparent in the high speed interconnect link. The smaller associated clearance land diameters can allow for better power distribution in the system.

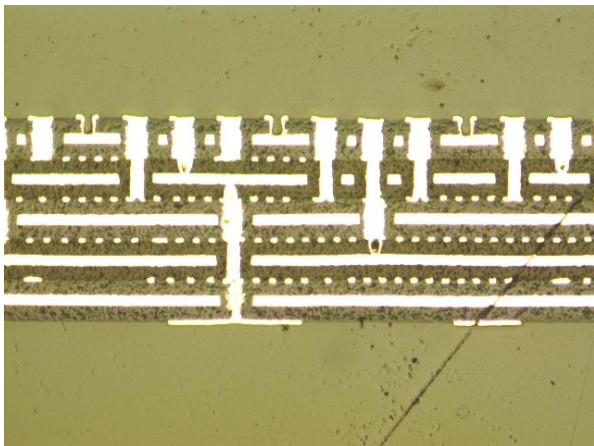


Figure 6: 150 C4 pitch semiconductor chip package, illustrating the density advantages of Full Z technology.

### III.B. Full Z Process and Materials

Processing of the two preferred basic building block structures (2S1P and 0S1P joining cores) are similar (Figure 7). Initially, clearance holes are etched in a free standing sheet of Cu. For the 2S1P, dielectric and Cu foil are then laminated to each side of the etched power plane. Through and blind vias, as required, are then drilled and plated and the signal layers are formed by subtractive etch processing methods. 2S1P structures are optically and electrically tested, as required, prior to Z-Interconnect joining. The 2S1P dielectric material can be glass cloth reinforced pre-preg or free standing material, such as resin coated Cu (RCC). The dielectric material choice within the 2S1P is virtually unlimited. The best reliability will be achieved when the dielectric material has a high glass transition (Tg) temperature and low Z expansion (CTE). 0S1P joining cores are formed by tack laminating the dielectric material to each side of the central Cu power foil. Holes are then drilled through the structure and filled with conductive paste. The dielectric material for the joining core is more critical than in the 2S1P. Like the 2S1P, high Tg / low CTE materials are preferred. Panasonic Megtron 6, Taconic TacPreg, i3 electronics eXaLam U, eXaLam H and eXaLam PPE RCC joining core dielectric materials have all been used successfully to date. High resin content pre-pregs or RCC's

Fabrication of coreless building blocks.....

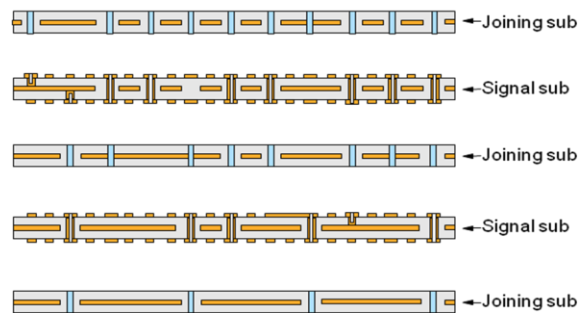


Figure 7: Full Z building block fabrication.

are preferred, and the thickness must be at least twice the thickness of the adjacent signal layers in order to assure void free composite structures. In the case of 0S0P joining cores, dielectric thickness must be at least twice the thickness of the combined copper thickness from both adjoining layers. For example, a 0S0P joining core that is to join signal layers on either side with 1 mil copper circuitry, the dielectric thickness in the joining core must be at least 4 mils (0.004") thick. Low melting point (LMP) alloy materials, such as



Ormet Circuits, Inc 701 paste, are preferred. Ormet 701 paste consists of eutectic SnBi and copper particles in an organic, fluxing, resin system. The SnBi melts at 138C to form a solid metal connection to the adjacent Cu pads, while continued lamination at 200C converts the majority of the joint to higher melt  $Cu_3Sn$  and  $Cu_6Sn_5$  intermetallic compounds. Some lower melt alloy material does remain in the joint, even after extended lamination time and temperature and multiple reflows, which serves as a self-healing medium of the buried via after multiple reflow cycles. Silver nano-particle pastes have also been effectively utilized in semiconductor chip package (SCP) applications, however, signal pads must be precious metal (Ag or Au) plated to form robust connections.

After completion of the various signal and joining cores they are aligned in a stack and laminated together, using the B-stage dielectric of the joining cores for bonding (Figure 8).

The laminated composite circuit board can be drilled and plated, as required, to accommodate compliant pin connectors and the like, although SMT type connectors are preferred from a density, performance and cost perspective.

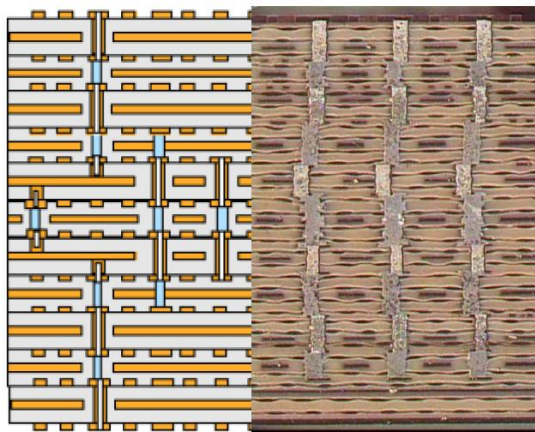


Figure 8: Schematic and corresponding photograph of a 23 metal layer z-interconnect substrate.

In addition to dielectric and conductive paste selection, several critical process parameters have been identified. Joining core dielectric tack lamination temperature, pressure and time are all critical to fill the power foil clearance holes, while not advancing the dielectric too much to limit composite lamination flow. Composite lamination parameters are also critical, as to determine correct timing between minimum viscosity of the resin system and the melt temperature of the conductive paste. Conductive paste fill of the joining cores is also important to insure solid material packing within the holes and consistent paste nubs on the surface (Figure 9).

IV. Current Induced Thermal Cycle (CITC) Test

Current Induced Thermal Cycle (CITC) Testing uses a DC current to heat a test net to a desired elevated test

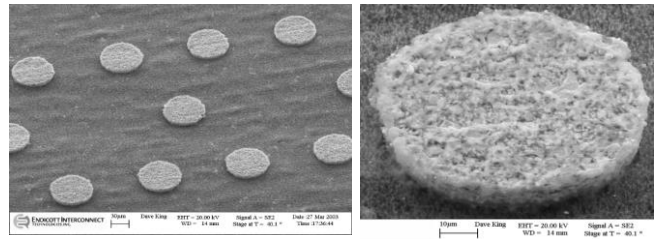


Figure 9: View of joining core paste nubs, ready for joining lamination.

temperature and then uses a fan to cool the coupon back to room temperature to make up one thermal cycle [3]. The test coupon consists of one net that serves as both the test specimen and the temperature sense net. The temperature of the net is determined from a resistance measurement based on a pre-established Thermal Coefficient of Resistance (TCR) for the particular net configuration on test (Figure 10). The test coupon is typically designed based on product attributes (e.g via and land dimensions, via pitch, etc.). The test net typically consists of 100 via stacks, daisy chained together with either external, internal or both, in 4 rows of 25 vias each. In the case of conventional PTH technology, the test coupon will be 100 vias, but for Full Z, test points could be in the several hundreds of joints – 100 via stacks times number of joining layers. Due to the compact nature of the combined test / monitor net, an entire coupon is less than 0.4” x 1.6” for a 1.0mm via pitch. This allows multiple coupons to be placed on a production panel, or for a development effort such as Full Z, a panel can be made up entirely of hundreds of CITC coupons. A standard CITC test cycle is from room temperature up to product reflow temperature (220C for Pb containing assembly or up to 260C for Pb-free reflow). Other thermal cycles are possible with CITC, such as ATC (0C – 100C) or DTC (-55C – 125C).

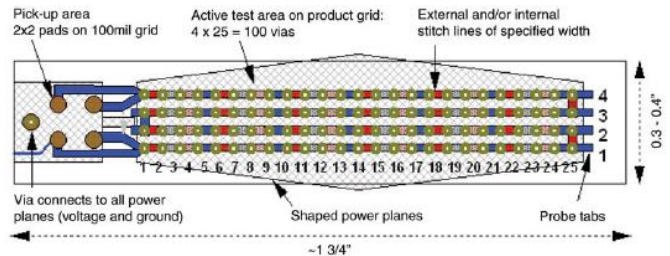
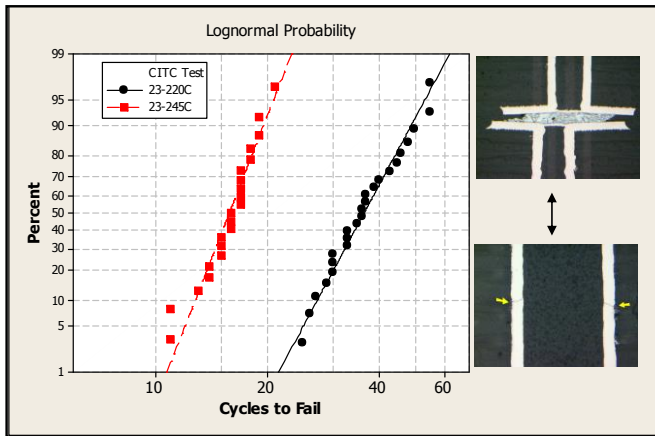


Figure 10: CITC test coupon configuration.

IV.A. CITC Test Results

Sub Z CITC test results are shown in Figure 11. Testing of this single joining layer product coupon was done at both

Pb containing (220C) and Pb-free (245C) reflow conditions. Sub Z test results are comparable to standard PTH technology, with both showing a dramatic reduction in interconnect life at the higher Pb-free reflow conditions. With cycling to 260C, life starts to approach 6 cycles for both conventional PTH and sub Z technologies. A desire is that a board be able to survive a minimum of four reflow cycles - one for SMT or wave solder each side and two more for rework, although rework is typically a localized heating. 6 cycles of CIRC testing provides a small safety margin beyond the typical assembly processing.

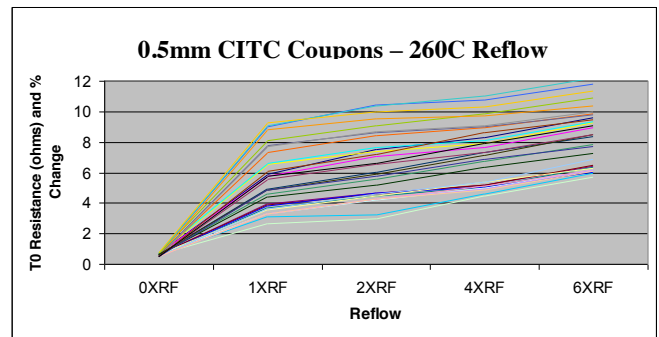
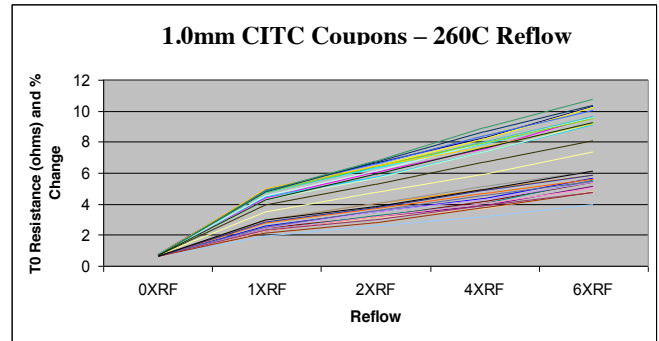


**Figure 11:** CIRC Cycles to fail at 23-220C and 23-245C Sub Z product. Failure analysis of the earliest fails shows that failure mode is in the buried vias, not the Z joint..

Full Z 260C reflow test results of 1.0mm and 0.5mm CIRC coupons are shown in **Figure 12**. Resistance change through 6X reflow cycles is approximately 10%, with approximately half the change occurring during the first cycle. There appears to be two different groups within the 1.0mm coupons – those with a 4-6% resistance change at 6X and those with an 8-11% change at 6X. This observation is real, in that the coupons with the 4-6% change contain 204 Z-I joints per coupon, while those in the 8-11% range contain 300 joints per coupon. Analysis of some of the coupons after 6X showed that some of the buried vias had experienced “knee” cracks during reflow, but that the Ormet paste had “healed” these cracks by filling with the higher than Cu resistivity Sn / SnBi / SnCu intermetallic materials. Many of these 6X reflowed CIRC coupons were subsequently tested at 23C-150C CIRC for 3000 cycles, without any resistance change.

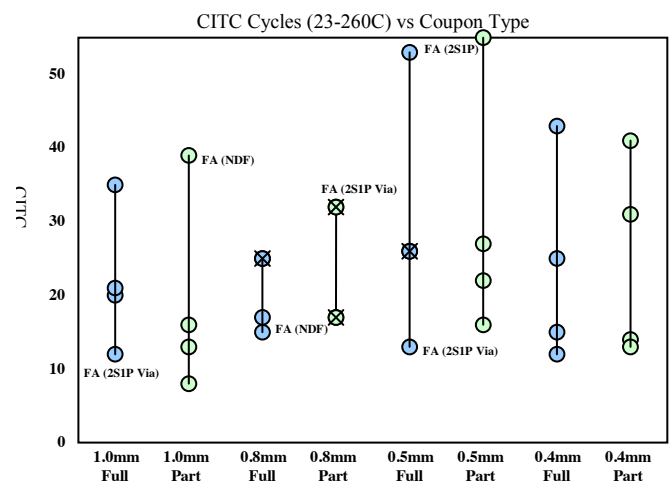
Full Z 260C CIRC test results are shown in **Figure 13**. All coupons survived a minimum of 8 to 50+ cycles of 260C CIRC testing. Failure analysis of several of the earliest fails, as well as some of the high cycle fails, showed either a barrel crack at the center of the buried via or a defect could not be found (NDF). The buried via cracks observed in CIRC testing, as well as the buried via “knee” cracks observed in reflow testing were actually due to poorly laser formed vias

and are easily corrected. The CIRC test results in Figure 15 have been broken out by via pitch (0.4, 0.5, 0.8 and 1.0mm)



**Figure 12:** Full Z CIRC Coupons with 6X – 260C reflow cycles. Many of above coupons were subsequently CIRC tested to 150C, 3000 cycles without further resistance change.

and by Full or Partial stack. A full stack is a top to bottom stack of Z-I joints and buried vias with 300 Z-I joints per coupon, while a partial stack includes some full stacks of Z-I joints and buried vias, but also stacks from either side to the middle, which results in 204 Z-I joints per coupon. There appears to be no significant difference in CIRC performance based either on via pitch or stack type.



**Figure 13:** Full Z 260C CIRC Cycle results by coupon type. Failure analysis of both early and late cycle fail coupons

showed either no defect or buried via failures.

## **V. Conclusion**

The converging, and often conflicting, needs for high density and high performance electronic package across the industry are driving the need for new technology. Previously employed technologies, such as HDI and back drill via stub reduction are becoming cost prohibitive and offer limited extendibility to future electronic packaging requirements.

The Full Z technology presented here offers density that is equivalent to or exceeds that of HDI technology, while simultaneously meeting the performance requirements for HPC applications. The work presented here also shows the ability of Full Z technology to meet the most demanding assembly and long term interconnect reliability demands. Full Z technology also appears capable of meeting continuing density and performance needs well into the future.

## **Acknowledgments**

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