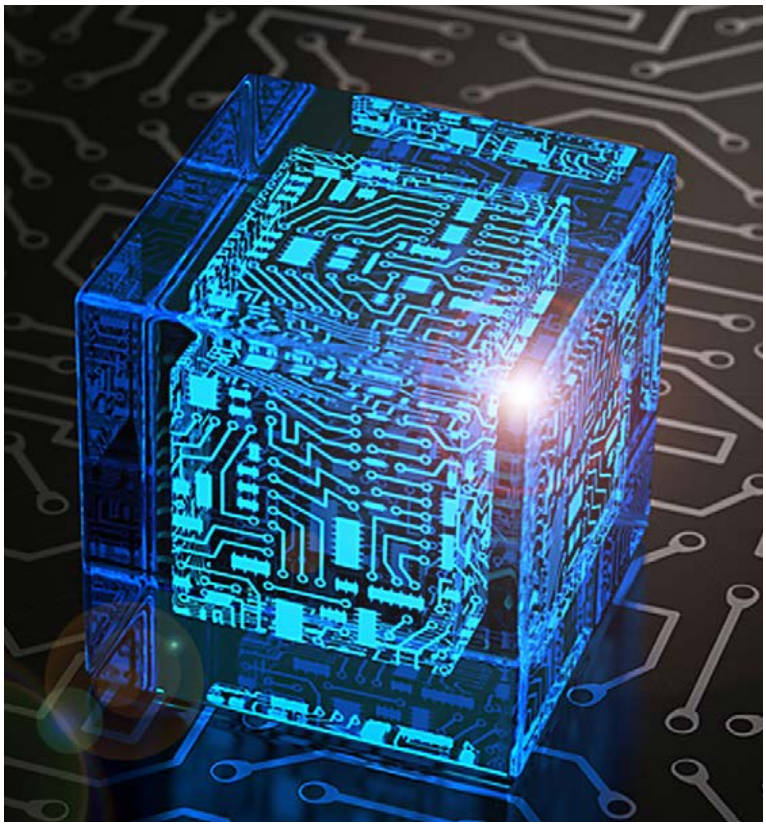
FEATURE

Building HDI Structures Using Thin Films and Low Temperature Sintering Paste



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Abstract

Circuit complexity and density requirements continue to push PCB fabrication capability limits. Component pitch and routing requirements are continually becoming more aggressive and difficult to achieve in good yield with current fabrication strategies. The trend is to bring the PCB closer to the density requirements required for semiconductor packaging. The ability to place interconnecting vias in any location on any layer is crucial to PCB fabricators in meeting this high density interconnect (HDI) trend.

The two fundamental elements in any type of PCB, conductors and dielectrics, both have to be considered when building "any layer" HDI. These PCBs have specific challenges for processing while maintaining thermal and electrical performance. Careful consideration of the interplay of the fundamental elements is critical to fulfilling all of these requirements.

New methods and materials designed specifically with these challenges in mind are becoming available for building HDI.

Using materials specifically designed for HDI PCBs can significantly reduce the challenges faced when producing these boards. However, along with easing the challenges of fabrication, these materials must also demonstrate the right combination of properties to meet electrical and thermal requirements while also being reliable. Validation of these new technologies is currently underway.

Background

Back in the day, just taking advantage of double-sided-clad increased density. Being able to route traces in the same location on each side of the PCB, interconnected with plated through holes, added significant density compared to a single-sided PCB (Figure 1). Logically, as chips became more powerful with more I/Os, adding layers became the natural progression.

However, HDI is not just about layer count. Adding layers has a diminishing return as the through holes and vias grab valuable real estate.

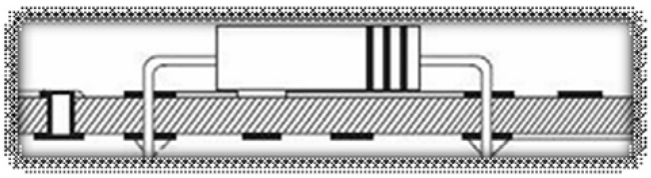

Figure 1.

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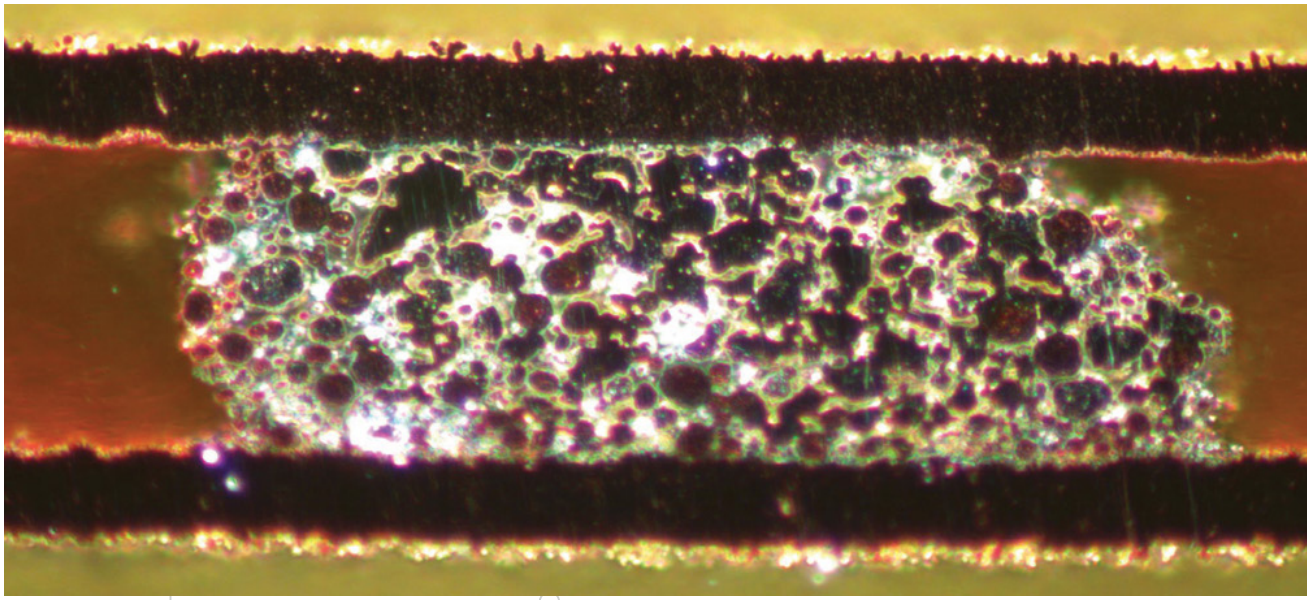

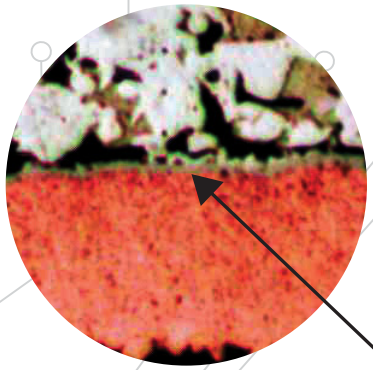

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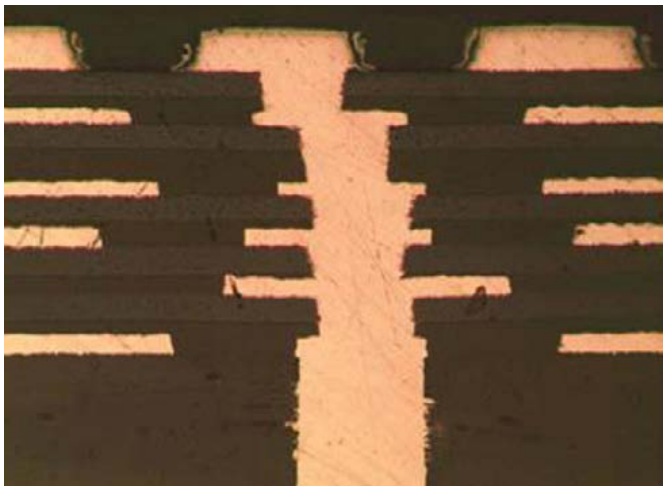

Figure 2: Sequential build-up.

Buried vias and "subs" provide an intermediate solution to higher density requirements, but these techniques greatly increase the process complexity and time in the PCB fabrication facility.

As the high density trend marched onward, build-up or sequential lamination became popular as laser drilling and better plating technology enabled blind microvias. Sequential build-up has the big density advantage of placing vias anywhere on any layer, but each layer has the process steps of an individual PCB. Lamination and plating capacity must be greatly increased to accommodate this solution (Figure 2).

There is a growing gap between cost-effective PCB manufacturing and HDI PCB requirements. New technologies—materials and methods—are needed for the industry to meet current and future demands.

Introduction

What if vias could be formed without plating? More importantly, what if the vias could be formed before lamination? If vias could be made this way, trips through plating and lamination can be greatly reduced. Making this possible would require the insertion of a conductor into vias in the dielectric layers between the individual circuit layers. This may be done several ways.

Some methods do this to C-stage (cured) dielectrics and some to B-stage (uncured) dielectrics. Ideally, the conductive material would be in liquid or paste form so it may be inserted into the vias after drilling, but before lamination. In applying the ink or paste, measures must be taken to ensure that the surface of the dielectric is not contaminated with conductive residue that can lead to electrical leakage, migration, etc.

Creating the interconnecting vias before lamination can greatly simplify the PCB manufacturing while still enabling via placement anywhere on any layer. In addition, formation of conductive vias prior to lamination may be combined with traditional processes for circuit formation and lamination, thus allowing the most efficient and cost-effective use of the PCB shop.

First Element: The Conductor

Sintered vs. Non-Sintered

Sintering refers to a process where a mixture of particles are fused together, usually thermally. Sintering mixtures can be used for structures and dielectrics, as well as conductors.

Conductive sintering products have been used in electronics for some time with ceramic thick film technology (cermet). Cermets require high temperatures (>800°C) for sintering and often ceramic substrates as the dielectric base material.

Non-sintering conductive pastes based on polymers, rather than ceramics, have been used with PCB materials as well as in printed electronics. These polymer thick film (PTF) materials are typically uncured liquid polymers, usually epoxy or acrylic based and filled with conductive particles. As the polymer cures and shrinks, the particles come in to contact with each other and the substrates making the connection (Figure 3).

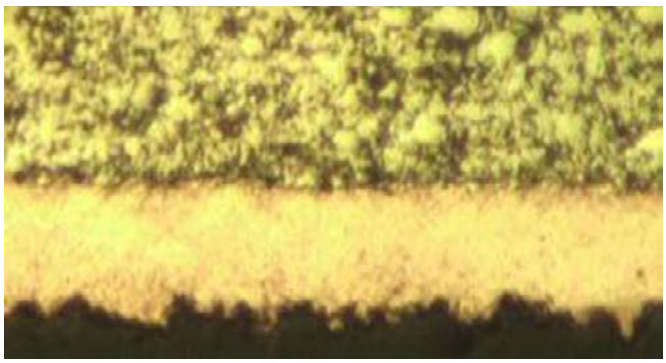

Figure 3.

PTFs have the benefit of low cure temperatures and are compatible with all kinds of polymer substrates. Two challenges with PTFs are changes in conductivity due thermal expansion and oxide on the surface of the individual particles. Silver is a popular choice for the latter because its oxide is reasonably conductive.

Sintered Interconnect Matrix Components	Melting Point (°C)	Percentage of Matrix
Cu	1085	>85%
Cu6Sn5	415	
Cu3Sn	640	
Bi	271	< 15%

Table 1.

The resistance behavior of PTFs is altered by temperature changes in reliability testing as well as in-service conditions. The need to pass traditional reliability testing therefore makes it challenging to implement PTFs in Z-axis interconnects.

Transient Liquid Phase Sintering

TLPS (transient liquid phase sintering) takes advantage of the fact that a liquid metal (e.g., tin) will interdiffuse with a non-molten metal (e.g., copper) to form a solid metallurgical joint at relatively low temperatures. This type of interdiffusion—in this case between copper and tin—results in a metallurgical bond between the two metals that is stronger than a mere layer-to-layer interface.

Interdiffusion between metals has long been used in electronic assembly to create strong, environmentally robust electrical interconnects. Solder joints of all kinds rely on a copper/tin diffusion and intermetallic formation to provide a strong, lasting bond.

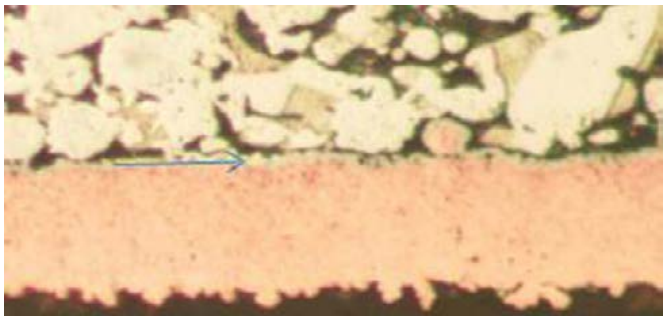

Figure 4: TLPS interconnects that provide a continuous metallurgically bonded electrical pathway.

A conductive paste may be formulated with TLPS characteristics so that sintering of the metals in the paste is possible at normal PCB laminating temperatures (as low as 180°C). The use of tin in such a TLPS paste has the added benefit of forming metallurgical bonds not just through the bulk of the paste interconnect, but also with the copper foil circuitry—just like solder would (Figure 4). However, unlike solder, the TLPS paste will not wet beyond the vias footprint and will not remelt during subsequent processing. Thus, the TLPS-paste-filled-via metallurgically ties the circuit layers in the Z-axis during standard lamination conditions. Like plated vias, TLPS paste interconnects provide a continuous metallurgically bonded electrical pathway.

Within the bulk of a TLPS paste via, copper and alloy particles "micro-weld" together to form a network of copper particles joined by copper-tin intermetallics and alloys. The remelt temperatures of the various phases are well above reflow temperatures and for all intents and purposes, non-reversible in the PCB (Table 1).

TLPS pastes can provide the via conductor stability necessary to enable a change in the PCB manufacturing sequence. Because the bonds are metallurgical and not just relying on particle contact, they have the ability to meet traditional electrical and thermal reliability requirements.

This opens many possibilities in PCB design and fabrication.

Second Element: The Dielectric

TLPS pastes have been used successfully with both C-stage and B-stage dielectrics. Using B-stage dielectrics have the benefit of creating

the Z-axis connections while bonding layers together. Of course a B-stage dielectric becomes a C-stage dielectric once laminated and cured. Consideration must be given to the flow characteristics of this layer for two important reasons. First, any resin that might flow and travel between the innerlayer copper foil surface and the TLPS paste before the intermetallic is formed will prevent the best possible interconnect. Second, flow of the resin may push the TLPS particles before they are locked in place. Successfully controlling these two characteristics comes from understanding and managing the process, but the right choice of materials can lead to high repeatability and high yields.

B-Stage Materials for TLPS Paste Z-Axis Interconnects

While flow of the B-stage resin may cause sintering issues, it is essential for layer-to-layer bonding. Loss of adhesion as well as lamination voids will cause issues in the PCB structure, and any successful HDI system must be free of these two defects.

Ideally, a B-stage material well suited for a TLPS interconnect would flow in the Z-axis only. This would allow bonding and in-fill between the copper circuits without pushing the paste around laterally before sintering. Such a material would be impossible to make; however, it is possible to manage the x-y flow and make very reliable connections.

Standard flow prepregs rely on the glass fabric for Z-axis thickness control and for resin retention to prevent voiding. They are the industry standard building block, even in HDI build-up methods.

Using standard prepregs with TLPS requires a greater understanding of their flow characteristics because of the potential for the prepreg resin to alter the shape or position of the TLPS-paste-filled-via as it flows. Things like heat rise and shelf life become even more critical.

HDI builds often require thinner, low glass/resin rich prepregs. This has the advantage of better laser drilling and better fill in fewer plies; however, the higher resin content has a disadvantage in the TLPS paste interconnect process. The higher proportion of resin exacerbates the flow problem. Not managed, the flowing resin can push the paste, even to the point of sweeping it away. Figure 5 shows a laser drilled, paste filled via before lamination. Note the gaps in the glass fabric.

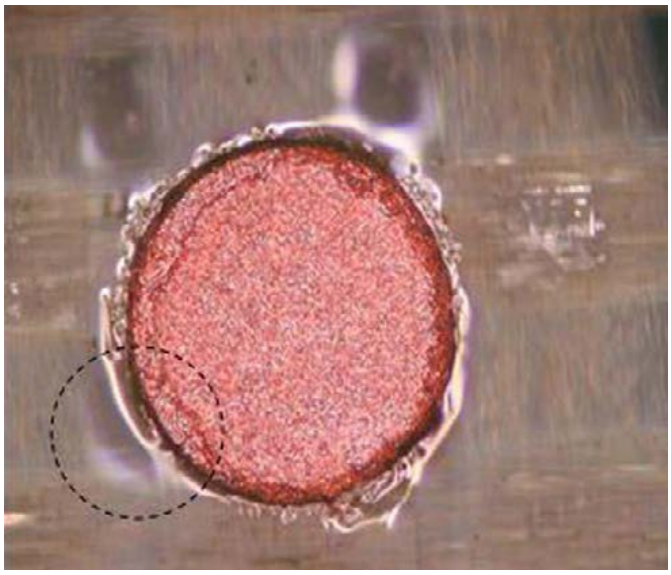

Figure 5: A laser drilled, paste filled via before lamination. Note the gaps in the glass fabric.

These areas are resin-rich and can move the paste in the via and potentially interfere with sintering quality and the formation of a continuous metallurgical network during lamination. In order to reduce the need to pre-engineer the process for suitable flow characteristics, no-flow prepregs may be substituted for standard prepregs in the TLPS paste via process. No-flow prepregs, more accurately called "very low flow" prepregs, do not rely on the glass as much for flow control. This offers better predictability in lamination and will help preserve the shape and position of the TLPS-paste-filled-via before sintering.

No-flow prepregs come in many different varieties from epoxy to polyimide, lead-free compatible and so on. These materials need to be studied individually for compatibility with both the fabrication process and the PCB requirements, but may offer many opportunities for straightforward implementation with TLPS interconnects.

Films for Tips Interconnects

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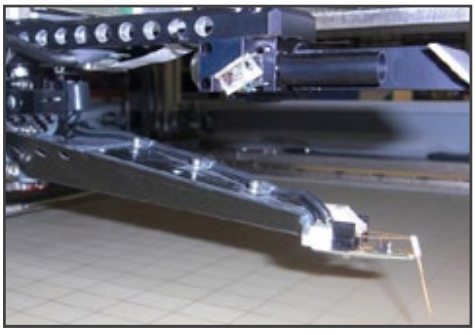

Basic specification	8 test probes, 4 XGA color cameras
Test area	610 mm x 510 mm
Smallest test point	35 µm (*with micro needle probes)
Repeatable accuracy	+/- 4 µm
Test voltage	up to 1000 Volts
4-wire Kelvin measurement	0,25 mΩ - 1 kΩ (± 0,1 mΩ ± 2 %)

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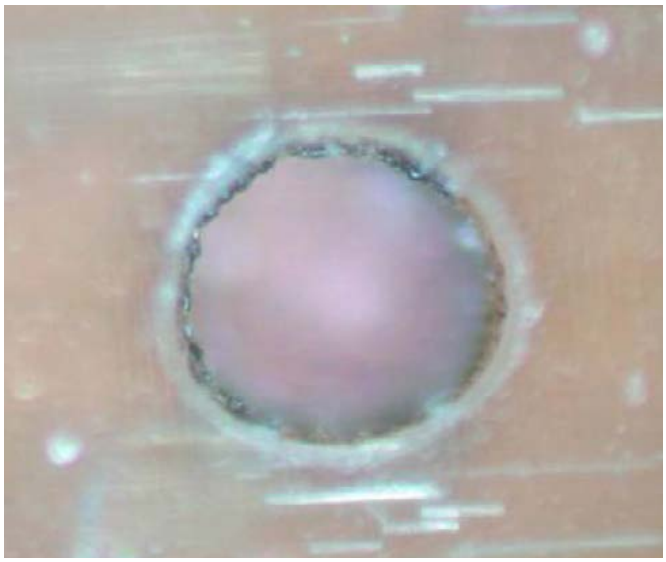

Figure 6.

Laser drilling B-stage materials is not normally done, but is required to take advantage of the pre-lamination via formation sequence. With glass fabric materials, the ends of the fibers tend to melt, forming "slag" droplets at the ends of the bundles (Figure 6).

Films tend to laser drill better, even in B-stage form. This is due to a uniform composition—all polymer instead of polymer plus glass. The type of laser used needs to be matched to the film as optically transparent films do not respond well to UV laser energy.

Many bonding films are available to the industry for flexible PCBs. These films are designed to be flow-reduced because it is common to machine the film prior to lamination. This kind of flow characteristic is very good for TLPS paste. Unfortunately, flex films contain one or more plasticizers which not only impart flexibility, but are integral to the flow control. Many plasticizers soften readily with heat and undergo large amounts of thermal expansion. Neither of these is desirable in HDI stack up structures.

Considering the requirements for HDI PCBs implementing TLPS interconnect, it is possible to develop a film without the plasticizers needed for flex. HDI PCBs are free from the dynamic bending requirement. This opens up some interesting formulation possibilities.

The new film concept is to replace the "rubberized" matrix with a polymer matrix that will behave more like the glass weave, but without the negatives. A proprietary high-temperature polymer is crosslinked to better mimic woven glass without the differential lasing characteristics, poor dielectric performance and resin wetting issues common to glass. This matrix is combined with a primary high-temperature B-stage resin with high bondability, long shelf life and will not advance during via formation and TLPS paste installation steps. This system can provide ease of use with interconnecting TLPS pastes, offering process latitude and thermal reliability.

By designing the dielectric film with both the paste interconnect process and the HDI PCB form-factors in mind, implementation of TLPS Z-axis interconnect becomes straightforward. The entire materials set has been designed to work together, with minimal impact to standard PCB manufacturing processes, and to support thin high-density PCBs with high electrical performance characteristics. With this film design, proper flow control of the resin can be tailored to the TLPS paste to maintain the unsintered paste in a well-defined via shape and not allow resin interference with the formation of a metallurgical bond to the copper pads (Figure 7). The interconnect is therefore dense, continuously metallurgically interconnected from pad to pad, and consistent from via to via.

The film system is not dependent on glass fabric, thermal aging, etc., for flow control, so the resin effect on the TLPS via is predictable and consistent over a long shelf life. Also, the film

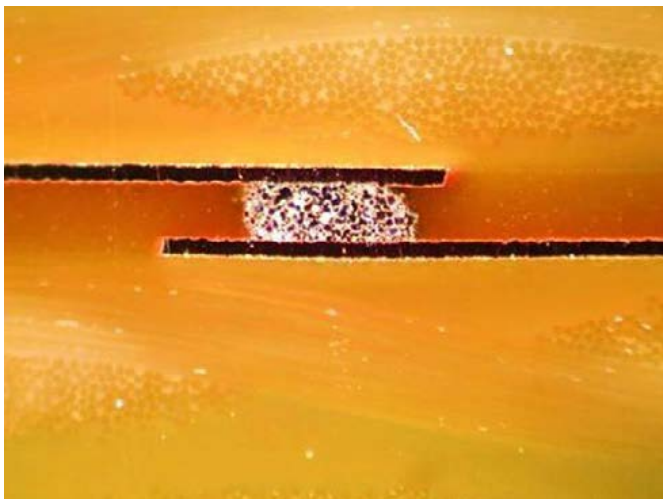

Figure 7.

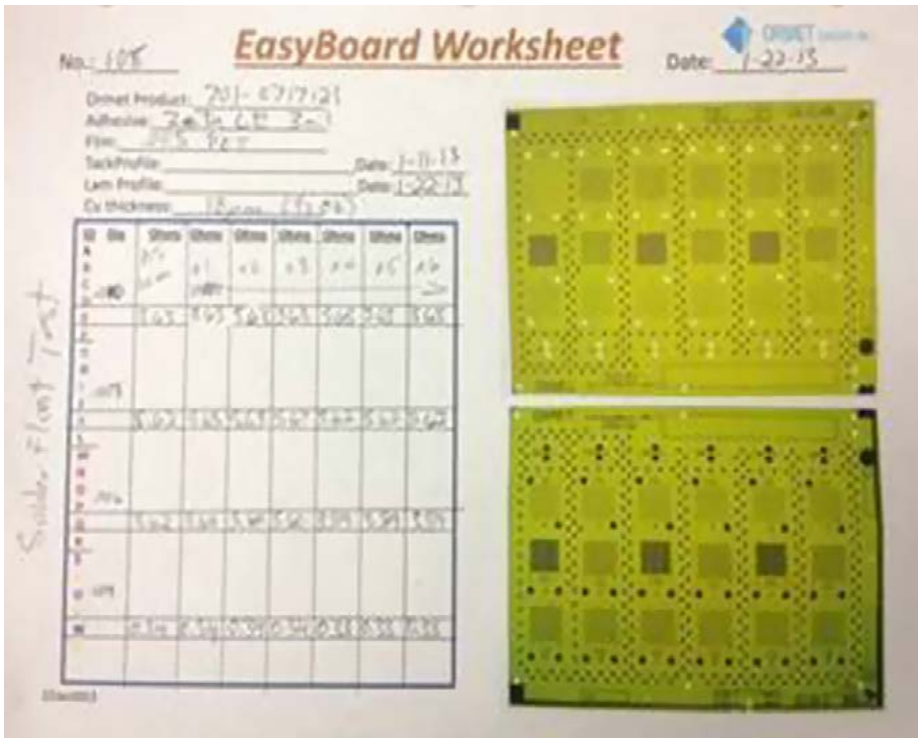

Figure 8: The effects of thermal shock on the TLPS Z-axis interconnects.

as copper plated and filled microvias.

This new film design was put into a test vehicle to examine the effects of thermal shock on the TLPS Z-axis interconnects (Figure 8).

Figure 8 shows some resistance measurements on a "daisy chain" test vehicle with six, 10-second solder floats at 288°C (Figure 10).

Also tested were 4, 6, 8 and 10 mils vias. 100% of the interconnects had very little or no change in resistance. The 4 mil via daisy chain was put back in the 288°C solder for a full minute and rechecked for resistance; again, there was no change. Figure 9 shows a continuous alloy formation with the copper foil at the bottom of the via.

is a stand-alone dielectric without the electrical performance and thickness constraints imposed by glass, but with thermal properties similar to a lead-free compatible glass reinforced system. The TLPS interconnects can therefore be short, in addition to the capability of placement anywhere in the PCB, and the overall structure can be very thin.

The intended result of this system approach is an HDI process that is less demanding on the PCB shop while providing the same reliability

Conclusion

Combing a TLPS paste with a film that is engineered without the constraints of flex can produce thermally reliable Z-axis interconnects. The TLPS paste offers a plating-like metallurgical bond to the copper innerlayers while the film allows proper sintering and controlled Z-axis expansion. Together, these materials give the PCB manufacturer ease of implementation of high-reliability sintered-paste interconnects and more construction options for HDI structures. **PCB**

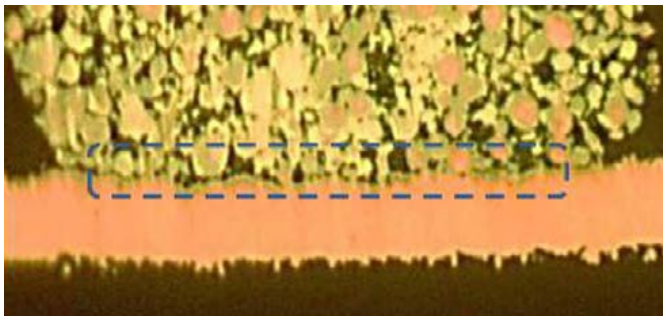

Figure 9: A continuous alloy formation with the copper foil at the bottom of the via.

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