ORMET CIRCUITS, INC.

Technical Data Sheet

Ormet 702

August 2013

PRODUCT DESCRIPTION

Ormet 702 is a thixotropic conductive paste used to create free-standing Z-axis interconnects by screen or stencil printing. Screen or stencil printed bumps of **Ormet 702** offer good shape retention after deposition and low resin bleed. The primary use for **Ormet 702** is to electrically join printed circuit board or IC package subparts into an integrated whole.

TYPICAL PROPERTIES

Property	Test Method	Value
Color 'As-received'	Visual	Copper color
Color 'Post-reaction'	Visual	Grey color[1]
Filler Type	Copper Filler and Tin Alloy Filler	
Nominal Particle Size	Hegman Gauge	< 20 microns
Viscosity (I)	Brookfield TE Spindle @ 5 rpm	530 kcps
Viscosity (II)	Malcom (10 rpm)	120 kcps
Thixotropic Index	Ratio of viscosity 1rpm / 10rpm	7
Approximate Specific Gravity		4.9 grams/cc
Electrical Resistivity	Volume Resistivity 4-point probe	50 μohm-cm
Thermal Conductivity	Laser Flash Diffusivity	25 W/mK
CTE	TMA expansion mode	22 ppm/°C
Lap Shear	Copper to Copper (0.125 in^2 overlap)	1500 psi[2]
Weight Loss on Cure	TGA	5%
Work Life	Application testing after RT storage	24 hours @ 25°C
Estimated Screen Life	Stencil print applications testing	8 hours
Estimated Storage Life		12 months < -10°C

[1] Surface may remain copper color if reacted in air or an atmosphere with sufficient oxygen to prevent fluxing of outer copper particles.
[2] SnPb solder paste tested as a control provided a value of 2200psi.

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TYPICAL APPLICATIONS

Ormet 702 is used to electrically interconnect substructures in printed circuit boards and semiconductor packaging. The use of **Ormet 702** enables HDI or high frequency portions of the electronic substrates to be manufactured independent from, and in parallel with, lower-cost conventionally–produced substrates, and then joined to form an integrated board assembly.

Applications for **Ormet 702** would include:

- Joining an HDI 'patch' to a conventional circuit board core
- Joining mixed-mode circuit boards (e.g. a microwave board to an HDI board)
- Creating electrically interconnected 3-dimensional cavity-type structures by joining via interposers to underlying circuit pads
- Attaching heat sinks

MATERIAL DEPOSITION GUIDELINES

Ormet 702 is applied by screen-printing or by stencil printing. The typical manufacturing process for joining circuit sub-assemblies with **Ormet 702** is to: deposit the paste on each sub-assembly, dry according to one of the profiles below, apply and register the overlying sub-assembly with the lower, and then cure in a lamination press according to one of the profiles below.

SINTERING PROCESS GUIDELINES[3]

	Recommended Profile	Alternate Profiles
Solvent Removal (Drying)	**60 minutes @ 95°C**	**30 minutes @115°C** **60 minutes @ 75°C**
Sintering	**60 minutes @ 190°C[4]**	**120 minutes @ 165°C[5]** **15 minutes @ 210°C**

STORAGE AND HANDLING

Ormet 702 is supplied in jars, syringes and cartridges. The storage temperature is [-10°C MAX]. Ormet 702 must be stabilized to room temperature for 30 minutes before opening the jars for use.

GENERAL INFORMATION

The Safety Data Sheet (SDS) contains safe handling information for this product. Please read carefully before handling or using this product.

The information provided in this Technical Data Sheet is believed to be correct and reliable; however, Ormet Circuits, Inc. does not assume responsibility for the user's implementation. Ormet Circuits, Inc. specifically disclaims all warranties expressed or implied including warranties for merchantability or fitness for use for a particular purpose, arising from sale or use of our products.

This product is covered by United States and foreign patents, both issued and pending, for the material compositions, applications and techniques for use. See the Ormet website for detailed patent information.

[3] Each application will require unique processing conditions; however, a lamination pressure of 300 PSI has been demonstrated to be effective in many applications.
[4] If voids are present after sintering, a 30 minute ramp from room temperature to the sintering temperature may reduce or eliminate the voids.
[5] The ultimate conductivity of Ormet materials may not develop at very low temperatures, but will improve upon brief thermal conditioning. A post-sintering thermal exposure above 210°C will develop its final properties.

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